Remarks

Favorable reconsideration of this application is requested in view of the following remarks. For the reasons set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The final Office Action dated June 21, 2004, indicated that claims 1-31 are rejected under 35 U.S.C. § 102(e) in view of *Lewchuk et al.* (U.S. Patent No. 6,298,424).

Applicant respectfully traverses the Section 102(e) rejection because the Office Action fails to present a *prima facie* case for maintaining a Section 102(e) rejection, and the cited reference fails to teach subject matter that corresponds to Applicant's claimed invention. The present invention is directed to a memory system that receives memory addresses corresponding to data in a particular order and rearranges the order by way of a control circuit that selects a memory reference from a set of pending memory references as claimed, for example, in claim 1.

With particular respect to the numerous claims and their respective limitations, the Office Action generally asserts that all of the claim features are taught without identifying evidence as to where the '424 reference includes such teachings and further ignores the limitations of the dependent claims by asserting that a discussion of such limitations "is not warranted at this time." This dismissal of Applicant's claimed limitations directly contradicts the requirements of 35 U.S.C. § 132 (The Examiner shall state the reasons for rejection together with such information and references as may be useful in judging the propriety of continuing the prosecution of the application.). This is also consistent with the purpose of aiding the Applicant in judging the propriety of continuing the prosecution, as indicated in 37 C.F.R. § 1.104(a)(2). While an ostensible attempt has been made to identify how the '424 reference corresponds to the claimed invention, the Examiner has failed to comply with this requirement. Applicant accordingly requests that the rejections be withdrawn.

More specifically and as a first example, the Office Action alleges that the control unit 46 of the '424 reference (Col. 9, lines 1-10) corresponds to the claimed control circuit; however, this cited portion of the '424 reference indicates otherwise. The "control unit 46" selects memory operations from request queue 44 in order; the control unit 46 does not select a memory reference from a set of pending memory references. The '424 reference teaches that the order of memory operations can be excepted when there is a higher priority

memory operation as assigned by the master. Thus, contrary to characterization in the Office Action, the '424 reference does not teach that the control unit 46 selects any memory reference from a set of pending memory references and/or with the references being presented to the memory array in a different order than that in which they were received.

Moreover, the Office Action has relied on the '424 reference for a Section 102(e) rejection by an interpretation that incorrectly characterizes "memory operations" from the '424 reference as memory references in a set of pending memory references per Applicant's claimed invention. This interpretation is erroneous in that the "memory operations" of the '424 reference have no relationship whatsoever to the memory references in Applicant's claimed invention; and the memory operations of the '424 reference are not used in any way analogous to Applicant's claimed invention. In the '424 reference a "memory operation" has to do with a microprocessor instruction, *e.g.*, read or write, involving data access via memory. In contrast, the memory reference of the claimed invention concerns addresses used by a memory to access particular memory cells, for example, during a read or write operation. *See* Applicant's Specification, *e.g.*, page 4, line 5 – page 5, line 21. The claims must be interpreted in view of the corresponding specification. MPEP § 2173.02.

With respect to claim 2, the Office Action fails to provide any correspondence to the teaching of the '424 reference. Further, the data buffer 50 of the '424 reference does not provide data from the DRAMs in the order received by the address buffer.

With respect to claims 3-7, the '424 reference does not characterize the DRAMs or main memory 14, as claimed. For example, column 9, line 30 *et seq.* provide a mode of operation that would correspond to the "interrupt" mode discussed above in connection with the reordering of memory operations (*see, e.g.,* Col. 9, lines 51-55).

Applicant's review of the '424 reference further reveals that the '424 reference fails to teach many of the claimed limitations of the remaining dependent claims. Some examples of such limitations are: a priority encoder (claim 8); a head pointer and a tail pointer (claim 9); a plurality of sequential cycles (claim 10); and a currently active row (claims 10-12). The Office Action erroneously relies on '424 teachings directed to a comparator at col. 10, lines 43-59 as corresponding to limitations directed to comparing a new address to the address of a currently active row. The '424 comparator however, merely teaches an interrupt operation wherein an interruption in the processing of pages of data allows for processing to resume where the processing left off on the page. There is no

discussion of comparison for priority purposes. Without a complete presentation of correspondence to each of the claimed limitations, the Section 102(e) rejection is improper and Applicant accordingly requests that the rejection be withdrawn.

With particular respect to claim 13 and dependent claims 14-19, the Office Action fails to allege any correspondence to limitations directed to "an out of order memory access request." Moreover, the '424 reference fails to teach an out of order memory access, as claimed. The '424 reference rather teaches an interrupt to a sequence of memory operations but fails to identify any out of order memory access. Applicant further fails to recognize how the Examiner would attempt to use the '424 reference as a basis for rejecting these claims depending from claim 13, for example, where the access occurs as a function of a state of the memory, as claimed. The Office Action fails to allege or present any correspondence to each of the claimed limitations; therefore the Section 102(e) rejection is improper and should be withdrawn.

With particular respect to claims 20-31, the Office Action fails to assert any correspondence between the '424 reference and limitations directed to prioritizing "as a function of data-access efficiency" and "before the received addresses are used to access the memory array." Applicant fails to recognize any teachings in the '424 reference that would correspond to the claimed prioritizing as a function of data-access efficiency. Specifically with respect to claim 22, the Office Action fails to assert, and Applicant fails to recognize, any teachings of the '424 reference directed to tracking states of accessibility, as claimed. With respect to claim 31, selection as a function of the state of the memory array has not been asserted by the Office Action and Applicant fails to see where the '424 reference teaches such limitations. Without a presentation of correspondence to each of the claimed limitations, the Office Action fails to present a *prima facie* Section 102(e) rejection and the rejection is improper. Applicant requests that the rejection be withdrawn.

In view of the above discussion, Applicant believes that the rejection has been overcome and the application is in condition for allowance. A favorable response is

requested. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is encouraged to contact the undersigned at (651) 686-6633.

Respectfully submitted,

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